Performance Analysis of an ATM Switch with Multiple Paths *

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Abstract

An ATM switch based on multistage interconnection networks with multiple paths can support higher bandwidth than that of buffered networks with single path by passing multiple packets to the same destination simultaneously. These multiple packets are buffered in the output buffer of the destination. The performance of output buffer in the switch with multiple paths is closely dependent on the output traffic distribution, which is the packet arrival rate at each output link destined to a given output port. As the nonuniformity of the output traffic distribution becomes higher, the performance of the output buffer as like delay and packet loss probability gets better. In this paper, we propose a new self-routing switch architecture with multiple paths called Fly network *and analyze the performance of the switching network and the output buffer focusing on the output traffic distribution. It is shown that the Fly network supports best throughput and latency of the output buffer by producing a high degree of the nonuniform output traffic distribution.*

1 Introduction

Asynchronous Transfer Mode (ATM) has been widely accepted as the transport and switching mechanism for future broadband networks [1, 2]. The performance of an ATM network is closely tied to the performance of the packet switches used [3]. In designing a high performance and large scale packet switch, one of the general approaches is to employ the nonblocking network providing multiple paths based on Multistage Interconnection Networks [4, 5, 6]. A packet switch with multiple paths provides multiple disjoint paths between each input and output, and therefore can transmit multiple packets to the same destination in a time slot simultaneously. These packets are buffered in the output buffer of the destination.

The performance of the output buffer under a certain fixed size is determined by two factors: the number of output links destined to an output and the *output traffic distribution*, which means the packet arrival rate at each output link. The output traffic distribution is nearly independent on the input traffic pattern offered to the switching network, but is dependent upon the particular switch architecture. For example, even if the input traffic pattern is random and uniform, many switching networks with multiple paths such as the tandem banyan switch [7] or multistage shuffle network [8] produce nonuniform output traffic distributions and the degree of the nonuniformity varies also with the different switching networks. As the nonuniformity of the output traffic distribution becomes higher, the performance of the output buffer as like delay and packet loss probability gets better [3, 9].

In this paper, we propose a new switch architecture called *Fly network* which can provide best performance of the output buffer by producing a high degree of the nonuniform output traffic distribution. The proposed switch architecture is based on the notified principle that a k by $k+1$ switching element is nonblocking itself, in which only two outlets are used for normal destination tag routing and the other $k-1$ outlets are used for rerouting. Such a k by $k+1$ switching element has no necessity for embedding internal buffers and this simplicity of the unbuffered switching element is a better candidate for fast VLSI technologies.

By the performance analysis, it is shown that the Fly network can support best performance of the output buffer producing a high degree of the nonuniform output traffic distribution close upon the ideal case. Other attractive features of the proposed architecture include a small and constant packet delay in the switching network less than $2log_2N$ and the guarantee of a first-in first-out packet sequence.

The remainder of this paper is organized as follows. In Section 2, we describe the design principles and the architecture of the Fly network. In Section 3, we analyze the performance of the switching network and the output buffer according to various output traffic distributions, and also illustrate the switch complexity of the Fly network. Finally, in Section 4 we state our conclusions.

2 The Fly Network Description

2.1 Design Principles

A major source of performance degradation in a MIN with single path is an *internal blocking* caused by a link conflict. In a general k by k switching element, the packet loss by the internal blocking is unavoidable

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within the switching element itself. The representative approaches to resolve the internal blocking are a buffered scheme [4, 10] and a multiple-paths scheme [5, 2]. In a buffered design, each switching element requires additional cost for buffers. The multiple-paths scheme is to provide more than one path between each input and output. When an internal blocking occurs in a switch with multiple paths, it is resolved by providing alternative paths for blocked packets rather than buffering.

Many switch architectures with multiple paths have been proposed to achieve high performance by taking advantages of multiple paths [7, 5, 11]. However, most of them pay for additional burdens to manage multiple paths such as lack of self-routing capability [5], tagging informations [7], and a long and variable packet delay [7, 11]. We present a new interconnection scheme for an ATM switch with multiple paths preserving the self-routing facility of the MIN and the small and constant delay. First, we make the following simple but crucial observation.

Property 1
(*Principle of k by k + 1 switching element*).
If a switching element consists of k by $k+1$, for $k \geq 1$, in which only two outlets are used for destination tag routing and the other $k-1$ outlets are used to provide a chance to be rerouted, then there is no internal blocking.

The proof of above property can be started from the blocking of a 2 by 2 switching element, in which if two input packets are destined to a same outlet, a packet is routed to the correct direction, but the other packet should be blocked. However, if one extra outlet is added to the switching element making it 2 by 3, the blocked packet can be transmitted through the extra outlet, apart from how to progress the packet on the extra link. Therefore, in a k by $k+1$ switching element, if we assume that only two inlets and two outlets are used for destination tag routing just like in delta class networks, and the remaining $k-2$ inlets and $k-1$ outlets are used as the extra links, then although all of k packets entering into k inlets are destined to a same outlet, all $k-1$ packets except one that is routed correctly can be processed through the $k-1$ extra links, called *alternative links.*

To preserve the self-routing and non-blocking property of the k by $k+1$ switching elements in a switching plane like a banyan network consisting of k by $k+1$ switching elements, each $k-1$ alternative outlet should be connected to different switching planes. Following property states the minimal configuration of the k by $k+1$ switching element to interconnect multiple switching planes.

Property 2
(*Minimality of 3 by 4 switching element*).
The minimal configuration of the switching element to interconnect multiple switching planes consisting of k by $k+1$ switching elements preserving their nonblocking property is 3 by 4.

First, considering a few switching planes such as the banyan networks consisting of 2 by 2 switching elements, it is simple that at least an alternative link per each switching element is required to interconnect two different switching planes for vertical direction, named spl_1 and spl_2. In the upper layer's switching plane, i.e., spl_2, each switching element requires then two additional outlets, making it 3 by 3+1, and these two alternative outlets must be connected to the different switching planes each other, named spl_3 and spl_4. Similarly, in spl_3, its two alternative outlets are connected to spl_5 and spl_6, and spl_4 requires also spl_7 and spl_8. Figure 1 shows an example of the interconnection scheme by alternative links, in which three 3 by 4 switching elements must be involved in three different switching planes each other.

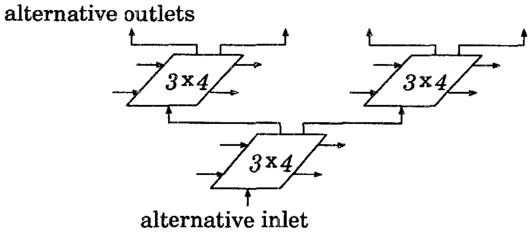


Figure 1: An example of the interconnection by the alternative liks.

2.2 Switch Architecture

The Fly network consists of multiple switching planes connected in the three dimensional direction (Figure 2). A switching plane, referred as *FPL(l, p)*, is a *l-banyan* (a banyan network without the initial $[l-1]$ stages, where $[x] = x$ if $x \geq 0$ and $[x] = 0$ if $x < 0$), which located in the lth layer vertically arranged and the pth plane horizontally arranged in that layer; in such a way, the switching planes in the lowest layer, i.e., layer *0* and the layer *1*, are complete log_2N stages banyan networks, and the banyan networks on the highest layer consist of only one stage (i.e., the log_2N*-banyan*).

We describe a switching element in an $N \times N$ Fly network as SE[*FPL(layer, plane), stage, loc*], where symbols are defined as follows,

$$\begin{aligned} layer &: 0 \sim log_2N, \\ plane &: 0 \sim 2^{[layer-1]} - 1, \\ & \qquad where \ \ [x] = \begin{cases} x & \text{if } x \geq 0 \\ 0 & \text{if } x < 0 \end{cases} \\ stage &: [layer-1] \sim log_2N - 1, \\ loc &: 0 \sim \frac{N}{2}. \end{aligned}$$

There are three types of switching element, i.e., a SE[*FPL(layer, plane), stage, loc*] is 1 by 2 if $stage = layer - 1$ and $layer \geq 1$, 2 by 3 if $layer = 0$, and 3 by 4 in other case, i.e., if $layer \geq 1$ and $stage \geq layer$. Most switching elements are 3 by 4.

In a 3 by 4 switching element, one alternative inlet is connected from a switching element in the lower

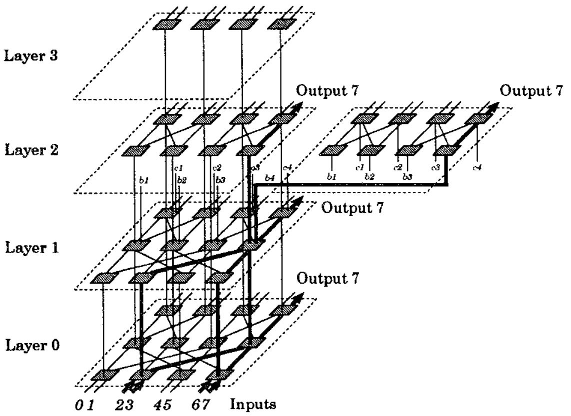


Figure 2: An 8 × 8 4-layered Fly network and the routing example.

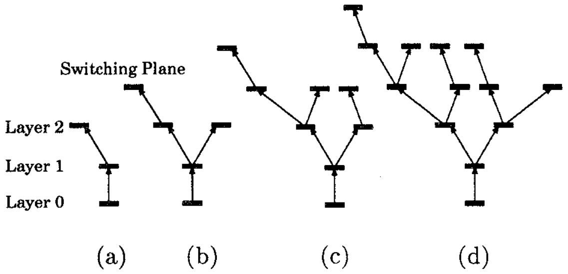


Figure 3: Abstract views of k-layered Fly networks : (a) 3-layered, (b) 4-layered, (c) 5-layered, and (d) 6-layered Fly network.

layer and two alternative outlets are connected to upper layers. For instance, SE[*FPL(layer, plane), stage, loc*] is connected to SE[*FPL(layer* + 1, 2 · *plane),stage,loc*] and SE[*FPL(layer* + 1, 2 · *plane* + 1*),stage,loc*], respectively.

From the number of layers in a Fly network, we refer it a *k-layered* network which consists of k layers numbered from layer 0 to layer $k-1$. In a k-layered network, the total number of switching planes, referred $\mathcal{L}_k$, means directly the number of multiple paths supported between each input and output port. Therefore, an output port can accept up to $\mathcal{L}_k$ packets arrived from $\mathcal{L}_k$ switching planes in a time slot and these packets are buffered in the output buffer. For example, $\mathcal{L}_k$ in a 4-layered network as shown in Figure 2 is 5.

To avoid the exponential increase of the number of switching planes as the layer becomes higher, we present a conflict resolution scheme with priority. When two packets for the same direction conflict in a switching element, a packet is routed to correct direction and the other packet is routed vertically only through the left alternative outlet. Accordingly, the traffic along the right upper switching planes is much less than that of left upper switching planes. If we consider a switching plane and the batch of vertical links between two switching planes as a node and an edge in a binary tree respectively, the k-layered Fly networks can be represented as Figure 3. The 1-layered network is identical to the original banyan network. Such binary trees are called Fibonacci trees [12] with an augmented root. By the definition of Fibonacci tree, the number of switching planes, $\mathcal{L}_k$, in a k-layered network is obtained by the Fibonacci sequence :

$$\mathcal{L}_k \quad = \quad F_k \quad for\ F_i = F_{i-1} + F_{i-2},\ i \geq 2, \qquad (1)$$

where $F_0 = F_1 = 1$. The number of layers in a Fly network can be chosen appropriately to the requested packet loss probability. The only source of packet loss occurs in the planes on the upper most layer.

2.3 Packet Routing

The packet routing algorithm in the Fly network is the same as the destination tag routing scheme used in general banyan networks. On each switching plane, all packets are routed to the output ports in parallel and in forward direction following the binary representation of the destination addresses. When two or three packets for the same direction conflict in a switching element, packets except one that is routed to the correct direction are routed through the alternative outlets. Because each switching element connected by alternative outlets is located in the identical position in upper switching planes, a packet transmitted to the upper switching plane can be rerouted without any loss of the previous routing history, but only with delay of one time slot. Figure 2 shows an 8 × 8 4-layered Fly network and the routing example. The thick links illustrate four disjoint paths for the four packets arrived in the 2nd, the 3rd, the 6th, and the 7th input port respectively, all of them are destined to the 7th output port simultaneously. If a conflict occurs in a switching element, a packet is correctly routed in the same switching plane and the remaining packets are routed to the upper switching planes through the alternative outlets (i.e., vertical links in the figure).

3 Performance Analysis

In this section, the throughput of the switching network and the output buffer of the Fly network are analyzed by the probabilistic model.

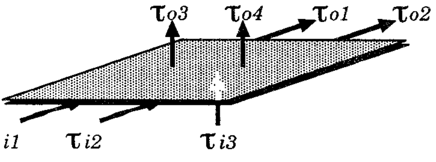


Figure 4: A 3 by 4 switching element.

3.1 Performance of Switching Network

The probabilistic model used here is similar to the analytic model by Patel [15]. To analyze with random request patterns, we borrow the following lemma regarding the statistical distribution of requests in a network operating under random request patterns [16].

Lemma : Let the packets be generated at the source nodes of the Fly network by independent, identically distributed random processes, that uniformly distribute the packets over all of the destination nodes. Then,

> **i)** The patterns of packet arrivals at the inputs of the same switch are independent.
>
> **ii)** Packets arriving at an input of a switch are uniformly distributed over the outputs of that switch.
>
> **iii)** For each stage in the network, the patterns of packet arrivals at the inputs of that stage have the same distribution.

For the conflict resolution scheme using alternative links, we add the following fourth assumption. Then,

> **iv)** The left alternative outlet has higher priority of packet transmission than the right one.

First, the state of each switching element is analyzed. Considering a 3 by 4 switching element as shown in Figure 4, each probability of four outlets is obtained by

$$\rho_{o1} = \rho_{o2} = 1 - (1 - \frac{\rho_{i1}}{2})(1 - \frac{\rho_{i2}}{2})(1 - \frac{\rho_{i3}}{2}), \quad (2)$$

$$\rho_{o3} = \frac{1}{2}(\rho_{i1} + \rho_{i2})\rho_{i3} + \frac{1}{2}\rho_{i1}\rho_{i2} - \frac{3}{8}\rho_{i1}\rho_{i2}\rho_{i3}, \quad (3)$$

$$\rho_{o4} = \frac{1}{8}\rho_{i1}\rho_{i2}\rho_{i3}. \quad (4)$$

According to the priority-based routing scheme, the right alternative outlet with ρ_{o4} is used only if a 3-conflict occurs, while ρ_{o3} for the left alternative outlet includes the probability of the 2-conflict as well as the 3-conflict. Applying the above equations to the whole switching network recurrently, we can obtain the throughput of the Fly network.

Figure 5 shows the packet loss probabilities of k-layered Fly networks under uniform traffic pattern with 90 percent load. In case of the 6-layered network consisting of 13 switching planes, the packet loss probability with $N = 2^{10}$ is 5.7×10^{-9}. Figure 6 shows the maximum throughput without output buffer. Because the output traffic distribution on multiple output links in the Fly network is nonuniform, while it is uniform in the crossbar switch, the throughput of the Fly network is better than the crossbar. Such a result is already noticed by Liew [3]; in his paper, it is shown that any nonuniform traffic pattern must result in performance close to or better than that of uniform traffic. Table 1 illustrates the output traffic distribution on each 13 output link in the 6-layered Fly network obtained by the same process used for Figure 6.

In Figure 7, we show the packet loss probability versus k at full load for k-layered Fly networks (N ranging from 32 to 1024). For a packet loss probability less than 10^{-6} for various N under full load, the 6-layered one is necessary.

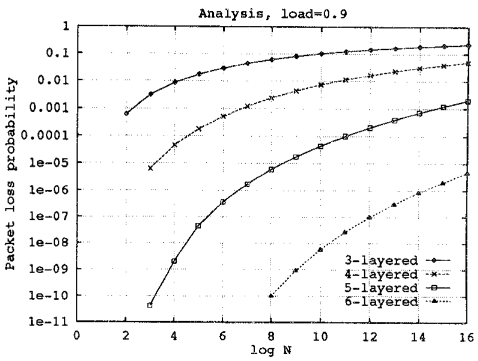


Figure 5: The packet loss probability of k-layered Fly networks under uniform traffic pattern.

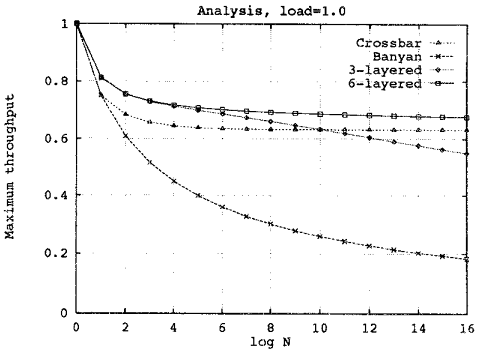


Figure 6: Maximum throughput under the uniform traffic pattern.

3.2 Performance of Output Buffers

The performance of the output buffer can be regarded as a function of the number of output links and the output traffic distribution at the output links. In this section, we propose an analytical model for the output buffer analysis, which is not dependent upon a particular switch architecture but applicable to the general switches with multiple paths.

3.2.1 Output Buffer Analysis

First, let us define several parameters related to the the output traffic distribution :

$\mathcal{L}$: The number of output links destined to an output.

$\mathcal{T}(i)$: The packet arrival rate on the ith output link, for $1 \leq i < \mathcal{L}$.

$\alpha(i)$: The probability of having i packet arrivals at a time slot all destined for a given output, for $0 \leq i \leq \mathcal{L}$.

layer	plane			
	0	*1*	*2*	*3*
5	9.0×10^{-5}			
4	1.3×10^{-2}	7.5×10^{-5}	2.0×10^{-6}	3.0×10^{-9}
3	1.2×10^{-1}	1.6×10^{-3}	6.6×10^{-5}	1.1×10^{-8}
2	2.7×10^{-1}	6.8×10^{-3}		
1	3.1×10^{-1}			
0	2.5×10^{-1}			

Table 1: The output traffic distribution of 6-layered Fly network with $N = 2^{10}$ and 100 percent load.

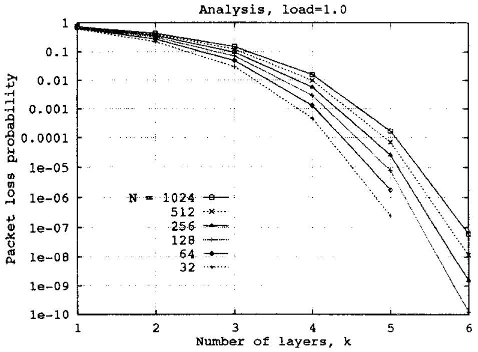


Figure 7: The packet loss probability versus the number of layers under the uniform traffic pattern.

Therefore, input arguments for the analysis of the output buffer are $\mathcal{L}$ and $\mathcal{T}(i)$. We model the output buffer as a discrete time Markov chain. With the buffer size of m, let Q_t denote the number of packets in a given output buffer just after the tth time slot, and A_t denote the number of packet arrivals during tth time slot, then,

$$Q_t \;=\; \min(\max(0,\ Q_{t-1} + A_t - 1),\ m). \tag{5}$$

Let Q denote the steady-state buffer size obtained from Q_t. Figure 8 shows the Markov chain state transition diagram. The transition probabilities are in terms of $\alpha(i)$. Then, $\alpha(i)$ for the nonuniform output traffic distribution is obtained by

$$\alpha(i) \;=\; \sum_{\Omega(\mathcal{L},i)} \left(\prod_{j=1}^{\mathcal{L}} \mathcal{T}(j)^{\omega_j} \cdot (1 - \mathcal{T}(j))^{1-\omega_j} \right) \quad for \;\; 0 \le i \le \mathcal{L}, \tag{6}$$

where

$$\Omega(\mathcal{L}, i) \;=\; \{(\omega_1, \omega_2, \ldots, \omega_{\mathcal{L}}) \mid \sum_{j=1}^{\mathcal{L}} \omega_j = i,\ \omega_j = \{0, 1\}\}. \tag{7}$$

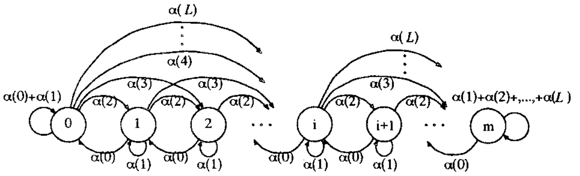


Figure 8: Markov chain state transition diagram of the output buffer.

However, in case of the uniform output traffic distribution, i.e., if all of $\mathcal{T}(i)$ are identical, $\alpha(i)$ has the binomial probabilities and is obtained by [13]

$$\alpha(i) \;=\; \binom{N}{i} \left(\frac{p}{N}\right)^i \left(1 - \frac{p}{N}\right)^{N-i} \; for \; 0 \le i \le \mathcal{L}, \tag{8}$$

where p is the offered input load. From the state transition diagram, we obtain the following balance equations.

$$\begin{aligned}
q_0 \simeq Pr(Q=0) \;&=\; (\alpha(0)+\alpha(1))q_0 + \alpha(0)q_1, && (9)\\
q_i \simeq Pr(Q=i) \;&=\; \sum_{j=0}^{i+1} \alpha(i+1-j)q_j \\
&\quad\; for \;\; 1 \le i < \mathcal{L}, && (10)\\
q_i \simeq Pr(Q=i) \;&=\; \sum_{j=(i-\mathcal{L}+1)}^{i+1} \alpha(i+1-j)q_j \\
&\quad\; for \;\; \mathcal{L} \le i < m, && (11)\\
q_m \simeq Pr(Q=m) \;&=\; \sum_{j=(m-\mathcal{L}+1)}^{m-1} \alpha(m+1-j)q_j \\
&\quad + \sum_{j=1}^{\mathcal{L}} \alpha(j)q_m. && (12)
\end{aligned}$$

Rather than using the Z transform of Q, we obtain the steady-state buffer size probabilities directly by the transition matrix for the Markov chain from above equations with the replacement of the last equation by

$$\sum_{j=0}^{m} q_j = 1. \tag{13}$$

The normalized throughput ρ is then [14]

$$\rho \;=\; 1 - q_0\alpha(0), \tag{14}$$

and the probability of the packet loss in the output buffer is

$$\begin{aligned}
&Pr[packet\ loss\ in\ output\ buffer] \\
&\;=\; \frac{1}{\lambda}\sum_{i=2}^{\mathcal{L}} \left(q_{m+2-i} \cdot \sum_{j=i}^{\mathcal{L}} (j-i+1)\cdot\alpha(j) \right) \\
&\;=\; 1 - \frac{\rho}{\lambda}, && (15)
\end{aligned}$$

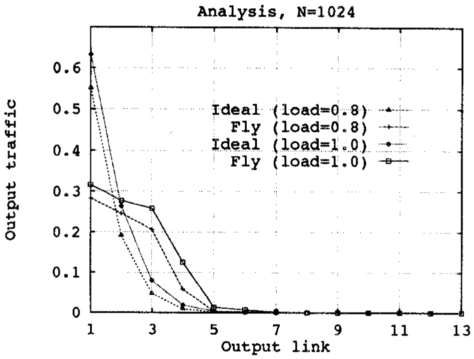


Figure 9: The output traffic distributions.

where

$$\lambda = \sum_{i=1}^{\mathcal{L}} \mathcal{T}(i). \tag{16}$$

The mean buffer length is

$$\overline{Q} = \sum_{i=1}^{m} i q_i \tag{17}$$

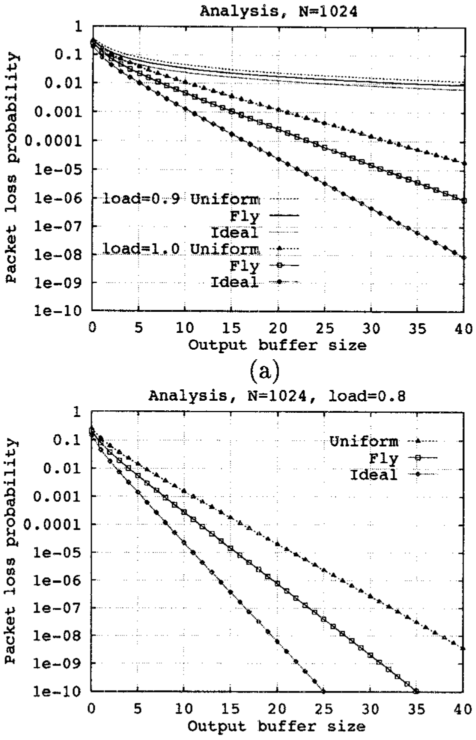
and the mean waiting time in the output buffer is obtained using the Little's formula as follows

$$\overline{W} = \frac{\overline{Q}}{\rho}. \tag{18}$$

3.2.2 Performance Results

Here, we show the analysis results of the output buffers. To compare the output buffer performance of the Fly network with other switches with multiple paths, we consider an ideal switching network providing multiple paths which can produce the most nonuniform output traffic distribution and also the case of uniform output traffic distribution. The output traffic distribution of the ideal switching network can be obtained by the probabilistic model used in the analysis of the Knockout switch [13, 5]. For instance, considering the first output link between $\mathcal{L}$ output links, we can assume that even if there is a packet destined to the output, the packet is to be passed always through the first output link. Accordingly, the second output link can deliver a packet when there are at least two packets destined to the output. Then, assuming that the input load is uniform, we can obtain each output traffic on the ith output link, $\mathcal{T}(i)$ by

$$\mathcal{T}(i) = 1 - \sum_{j=0}^{i-1} \left[\binom{N}{j} (\frac{p}{N})^j (1 - \frac{p}{N})^{N-j} \right] \quad for \ 1 \le i < \mathcal{L}, \tag{19}$$



(a)

(b)

Figure 10: The packet loss probability versus the output buffer size.

where p is the offered input load.

The output traffic distribution, $\mathcal{T}(i)$, of the Fly network is obtained by Equations (2), (3), and (4). Table 1 shows an example of $\mathcal{T}(i)$ in the 1024 × 1024 6-layered network under 100 percent load, in which $\mathcal{L}$ of the network is $\mathcal{L}_6 = 13$. In Figure 9, we plot each $\mathcal{T}(i)$, the output traffic distribution. We can observe that the output traffic distribution of the ideal switching network is more nonuniform than the Fly network. Figure 10 shows the packet loss probability versus the output buffer size obtained by the analytical model presented in the last section. To achieve the packet loss probability less than 10^{-9} for 1024 × 1024 switching networks with the 80 percent load, the Fly network requires 32 packet buffers, while the ideal switching network and the case of the uniform output traffic distribution require 23 and 44 packet buffers respectively. Such results are analogous to the analysis results of the output traffic distribution consistently, therefore, we can assert that the performance of the output buffer increases as the nonuniformity of the output traffic distribution becomes higher.

Figure 11 shows the mean delay versus the input load curve (obtained by Equation (18)) of the switching networks with the buffer size 40. The figure shows that all of the switching networks have small delay up to load 0.9 and the delay variance between the switch-

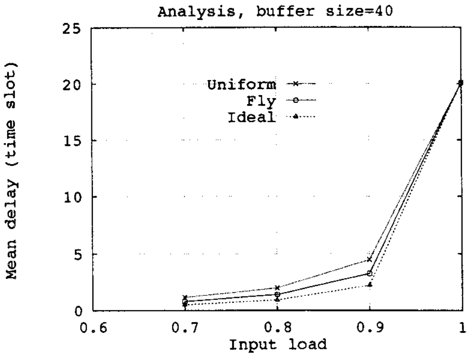


Figure 11: The mean delay versus the input load.

ing networks is very small.

3.3 Switch Complexity

In designing a large scale and high performance packet switch, the multiple-path scheme is the most robust one with respect to the switch simplicity and the guarantee of low blocking probability. However, many switching networks with this scheme suffer from high hardware complexity as the dimension of the switching network becomes larger. In this section we show that the proposed switch has nearly optimal hardware complexity compared with other switching architectures based on the multiple-path scheme.

As an approach to measure the hardware cost of a switching network, there is *crosspoints complexity* [18]. For an $m \times n$ crossbar switch its crosspoints complexity is represented as mn. In Table 2, we compute the crosspoints complexity of the 6-layered Fly network, the crossbar switch, the Knockout switch, and the 13-replicated banyan network, all of them provide at least 13 disjoint multiple paths. For an $N \times N$ crossbar, its crosspoints complexity is just $4N^2$ and for the 13-replicated banyan network it is $26N log_2 N$ [18]. In the Knockout switch, a concentrator in each output port requires about NL 2 by 2 switching elements, so its total crosspoints complexity becomes $4N^2L$ [13]. About the 6-layered Fly network it is limited to $54N log_2 N$, where $log_2 N \leq 16$. As shown in Table 2, the crosspoints complexity for the 6-layered Fly network with 13 switching planes is similar to the 13-replicated banyan network which has nearly minimal complexity to provide 13 multiple paths, while the performance of the Fly network is similar to the Knockout switch.

4 Conclusions

In designing a large scale and high performance nonblocking ATM switch providing multiple paths, the output buffer is the most important one which affects the whole switching system performance. The performance of the output buffer is determined by the number of output links destined to a given output and the output traffic distribution on the output links. This paper proposed a new switching network with multiple paths which can support a better output buffer performance by producing a high degree of the nonuniform output traffic distribution and an analytical model for the output buffer analysis with respect to the nonuniform output traffic distribution. It was shown that the performance of the output buffer increases as the nonuniformity of the output traffic distribution becomes higher.

Size, N	13-replicated Banyan	6-layered Fly	Crossbar switch	Knockout ($L = 13$)
256	53,248	80,128	262,144	3,407,872
512	119,808	188,672	1,048,576	13,631,488
1024	266,240	434,176	4,194,304	54,525,952
2048	585,728	982,016	16,777,216	218,103,808

Table 2: The crosspoints complexity of $N \times N$ switching networks.

To demonstrate the performance of the output buffer regarding the output traffic distribution, we considered an ideal switching network which can produce the most nonuniform output traffic distribution. By the performance comparison, we showed that the Fly network represents low packet loss probability of the output buffer close to the ideal switching network. Other attractive features of the proposed architecture include that: (a) better cost/throughput performance as the switch architecture has larger dimensions (e.g., $N \geq 2^8$); (b) low and constant packet delay; and (c) guarantee of a first-in first-out packet sequence.

Although not considered in this paper, this result is also applicable under nonuniform input loads such as a hot spot traffic or a bursty traffic. Because it is known that the performance in a nonblocking switching network is minimum under the uniform input traffic pattern [3], we may expect better output buffer performance under the nonuniform input traffic rather than under the uniform one.

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